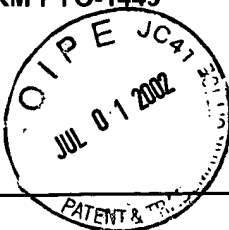


FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
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10/003,096INFORMATION DISCLOSURE
STATEMENT BY APPLICANTAPPLICANT
Steven D. RoachCONFIRMATION NO.
5186FILING DATE
December 6, 2001GROUP ART UNIT
2847 2821

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JV	3,573,644	04/06/71	Evel	330	9	
JV	5,121,075	06/09/92	Roach	330	126	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
JV	Addis, John, "Three technologies on one chip make a broadband amplifier", <u>Electronics The International Magazine of Electronics Technology</u> , June 5, 1972, pp. 103-107.
JV	Ahuja, B.K., "Implementation of Active Distributed RC Anti-Aliasing/Smoothing Filters", <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-17, No. 6, pp. 339-342.
JV	AMCC Product Brief 1.0/1.25GBPSVCSELDRIVER, May 10, 1999, pp. 1-3.
JV	Ikalainen, Pertti, K. "An RLC Matching Network and Application in 1-20 GHZ Monolithic Amplifier", <u>IEEE MTT-S International Microwave Symposium Digest</u> , Vol. I, 1989, pp. 1115-1118.
JV	Khoury, John, M., "Synthesis of Arbitrary Rational Transfer Functions in S Using Uniform Distributed RC Active Circuits", <u>IEEE Transactions on Circuits and Systems</u> , Vol. 37, No. 4, April 1990, pp. 464-472.
JV	Khoury, John, M., "On the Design of Constant Settling Time AGC Circuits", <u>IEEE Transactions on Circuits and Systems</u> , Vol. 45, No. 3, March 1998, pp. 283-294.
JV	Sackinger, Eduard, et al., "A 3GHz, 32dB CMOS Limiting Amplifier for SONET OC-48 Receivers", <u>IEEE International Solid-State Circuits Conference</u> , 2000, pg. 158.
JV	SUMMIT Microelectronics, Inc. "Dual Loop Laser Diode Adaptive Power Controller with Look Up Table" (SML2108), October 3, 2001, pp. 1-21.
JV	Swartz, R.G. et al., "An Integrated Circuit for Multiplexing and Driving Injection Lasers", <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-17, No. 4, August 1982, pp. 753-760.

EXAMINER

DATE CONSIDERED

02/07/03

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.